

A Step Response Based Mixed-Signal BIST Approach for Continuous-time Linear Circuits

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Abstract

A new Mixed-Signal Built-in Self-test approach that is based upon the step response of a reconfigurable (or multifunction) analog block is presented in this paper. The technique requires the overlapping step response of the Circuit Under Test (CUT) for two circuit configurations. Each configuration can be realized by changing the topology of the CUT or by sampling two CUT nodes with differing step responses. The technique can effectively detect both soft and hard faults and does not require an analog-to-digital converter (ADC) and/or digital-to-analog converter (DAC). It also does not require any precision voltage sources or comparators. This approach does not require any additional analog circuits to realize the test signal generator and sample circuits. The paper is concluded with the application of the proposed approach to a circuit found in the work of Epstein et al [1] and two ITC'97 analog benchmark circuits.

Keywords: Analog Built-in Self-Test, Mixed-Signal BIST, Analog test, Analog functional test

1. Introduction

The development of Built-In Self-Tests (BIST) for mixed-signal integrated circuits has been driven by the high cost associated with the production and field testing of complex mixed-signal VLSI circuits. A number of effective digital BIST techniques are currently available for implementing on-chip tests for the digital blocks of a mixed-signal circuit [2]. Unfortunately, this is not true for the analog blocks and the analog-digital interfaces between those blocks and digital circuits. Most of the current research in this area is primarily focused upon techniques to test these blocks and interfaces. Current analog/mixed-signal BIST techniques can be divided into two broad classes: (i) functional and (ii) fault-based [3]. In the functional approaches the analog block under test is driven with sinusoidal or multitone stimuli and measurements are obtained at the output or selected nodes [3,4,5]. This measurement data is subsequently processed with the DSP-core, in the ADC-DSP-DAC structure to detect system faults. Generally these techniques are based upon analog specifications like signal-to-noise ratio (SNR), frequency response or intermodulation distortion. The primary advantage of functional schemes is that they can detect both soft (or parametric) and hard faults [5]. These techniques are often considered to be the most effective because of this feature. Analog BIST techniques that employ fault coverage and fault detection base upon fault models of devices within the analog block or sub-

blocks are called fault-based techniques. The major advantage of these techniques is that they are typically implemented with nonconventional stimuli or signatures that can easily be generated and processed on-chip with digital techniques. However, these techniques can only effectively detect hard (or catastrophic) faults and discrete fault points in the fault space of the CUT.

A new functional analog BIST approach that does not require a ADC, DAC or complex DSP-core is presented in this paper. The technique is based upon a nonconventional input signal, i.e. a step function, that can detect both soft (or parametric) and hard faults over the entire fault space effectively without the large number of simulations (over all the potential failure modes of the CUT) typically required for BIST techniques that used these types of inputs. The technique also requires comparisons of the CUT outputs at several distinct fixed reference voltages. Hence, the test stimulus can be realized with a digital gate and the output sampling hardware with several CMOS inverters that have differing pMOS and nMOS device widths. The technique only requires n modified buffers, $2n$ registers (where n corresponds to the number of unknown parameters in the CUT) a digital counter and a simple single-bit processor core (or DSP); this processor can be realized by reconfiguring on-chip digital circuits. A single-bit core can be used to compute the parameters in the proposed technique because digital circuits are typically much faster

than analog circuits and only $n^2 + n$ evaluations are required per iteration of the Newton algorithm. The proposed technique is based upon the step response of the analog block under test (CUT).

The organization of the paper is as follows: the mathematical basis of the step response based BIST approach is presented in section 2. Examples of the application of the proposed techniques is presented in section 3. Our conclusions are presented in section 4.

2. Problem Formulation

The proposed Mixed-Signal BIST techniques is essentially a parameter extraction or system identification approach that is based upon the step response of a reconfigurable or multi-output analog circuit. The Newton-Raphson method is used to find the parameters

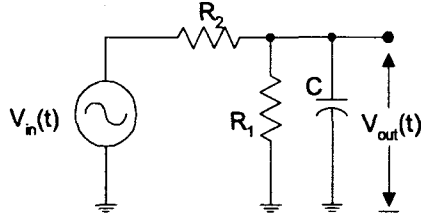


Figure 11 First Order Low-Pass Filter

of the CUT. The component functions used to construct the Jacobian matrix are functions of the CUT output voltage crossover point for two circuit configurations (i.e. the point in time where the CUT output exceeds a threshold or switching voltage), where the crossover point is determined by the threshold voltage of the logic gate that is driven by the CUT during BIST diagnosis.

Our primary objective in this section is to present the mathematical basis of this approach. The most effective way to do this is to apply the proposed approach to a simple circuit. The circuit selected for this demonstration, a passive first order high-pass filter, is shown in Fig. 1. The transfer function of this filter is,

$$H(s) = \frac{s + \alpha p}{s + p} \quad (1)$$

its pole and DC gain are,

$$p = -\frac{(R_1 + R_2)}{R_1 R_2 C} \text{ and } \alpha = \frac{R_2}{R_1 + R_2} \quad (2)$$

respectively. These relationships, i.e. equation (1) and (2), are determined by the circuit topology and the value of the circuit elements. We assume that circuit faults do not change the circuit structure therefore, the only parameters required to identify the system defined by equation (1) is p and α . The time-domain output $V_{out}(t)$ of this filter for a step function with a peak value of V_{DD} , i.e. $V_{in}(t) = V_{DD}\mu(t)$ is,

$$V_{out}(t) = V_{DD}[\alpha + (1-\alpha)e^{-\beta t}]\mu(t) \quad (3)$$

if we let $\beta = -p$. Now let's change the circuit topology as

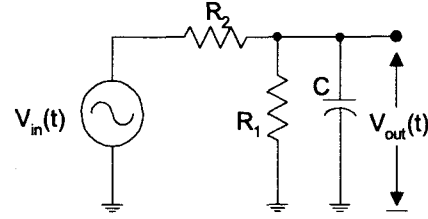


Figure 12 First Order Low-Pass Filter

shown in Fig. 2. The step response of this circuit in terms of α and β is,

$$V_{out}(t) = V_{DD}(1-\alpha)[1 - e^{-\beta t}]\mu(t) \quad (4) \text{ I f w e}$$

equate the output voltage of the two circuit configurations, i.e. eq (3) and (4), and rewrite that expression such that it equals zero we derive the following function in terms of α and β ,

$$f(\alpha, \beta, t_1, t_2) = V_{DD}\{2\alpha - 1 + (1 - \alpha)(e^{-\beta t_1} + e^{-\beta t_2})\} \quad (5)$$

The time t_1 and t_2 in the above function, i.e. eq (5), corresponds to the point in time where the output voltage of the circuit in Fig. 1 equals the output voltage of the circuit in Fig. 2. These time points, hereupon referred to as crossover points, correspond to the time when the output voltage of both circuit configurations equals a reference voltage V_{ref} . We will use the Newton method to find the above two parameters, i.e. α and β . Two sets of crossover points, i.e. (t_1, t_2) and (t_3, t_4) respectively, are required to realize the Jacobian matrix. The Jacobian matrix is,

$$J(\bar{x}) = \begin{bmatrix} \frac{\partial f(\alpha, \beta, t_1, t_2)}{\partial \alpha} & \frac{\partial f(\alpha, \beta, t_1, t_2)}{\partial \beta} \\ \frac{\partial f(\alpha, \beta, t_3, t_4)}{\partial \alpha} & \frac{\partial f(\alpha, \beta, t_3, t_4)}{\partial \beta} \end{bmatrix} \quad (6)$$

Now let us consider the above circuits, i.e. Fig. 1 and Fig.

2, for the following component values, $R_1 = 2K\Omega$, $R_2 = 1K\Omega$, $V_{DD} = 5.0$ volts, and $C = 100\mu f$. Then using eq. (3) we find that $\alpha = 1/3$ and that $\beta = 15.0$. The step response of Fig. 1 and Fig.2 for these values is shown in Fig. 3. If we let the reference voltages V_{Ref1} and V_{Ref2} equal 2.5 volts and 2.0 volts respectively, the crossover points are, $t_1 = t_2 = 92.41962$ mSec, $t_3 = 61.08605$ mSec, and $t_4 = 153.5057$ mSec. Now using the above crossover points and an initial

Table 1. The parameter values at the 7th iteration corresponds to the value of α and β in eq (4) for the above component values. The transfer function of the high-pass filter shown in Fig. 1 can then be computed as follows:

$$H(s) = \frac{s + \alpha\beta}{s + \beta} = \frac{s + 5}{s + 15} \quad (7)$$

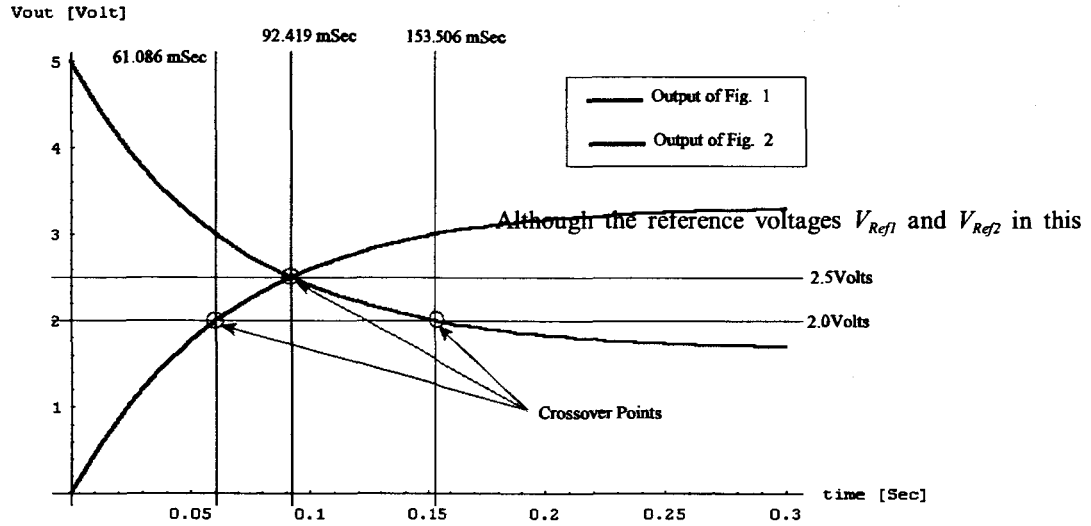


Figure 13 Output Voltage of above circuits

value of $\alpha = 0.1$ and $\beta = 25.0$ the Newton method converges rapidly (quadratically usually [6]) to the correct

example were set, their values in general are not required for the proposed approach. The only requirement is that

Table 1: Convergence Behavior of BIST Approach

Iteration	α	β	Error
0	.1000000	25.00000	.10000E+04
1	.2771510	6.68585	.18315E+02
2	.5621070	14.96517	.82842E+01
3	.3333337	15.01813	.23482E+00
4	.3333334	14.99999	.18145E-01
5	.3333333	15.00000	.10830E-04
6	.3333333	15.00000	.23894E-11
7	.3333333	15.00000	.00000E+00

they be set to two distinct values that insure that the Jacobian matrix is non-singular. Therefore, precision voltage references and comparators are not required to implement the proposed technique.

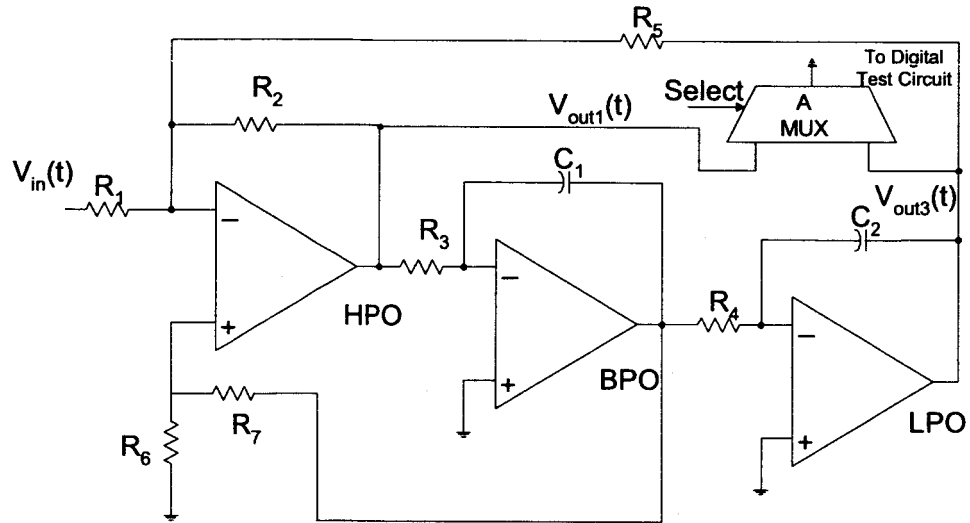


Figure 14 ITC'97 Continuous-Time State-Variable Filter

3. Examples

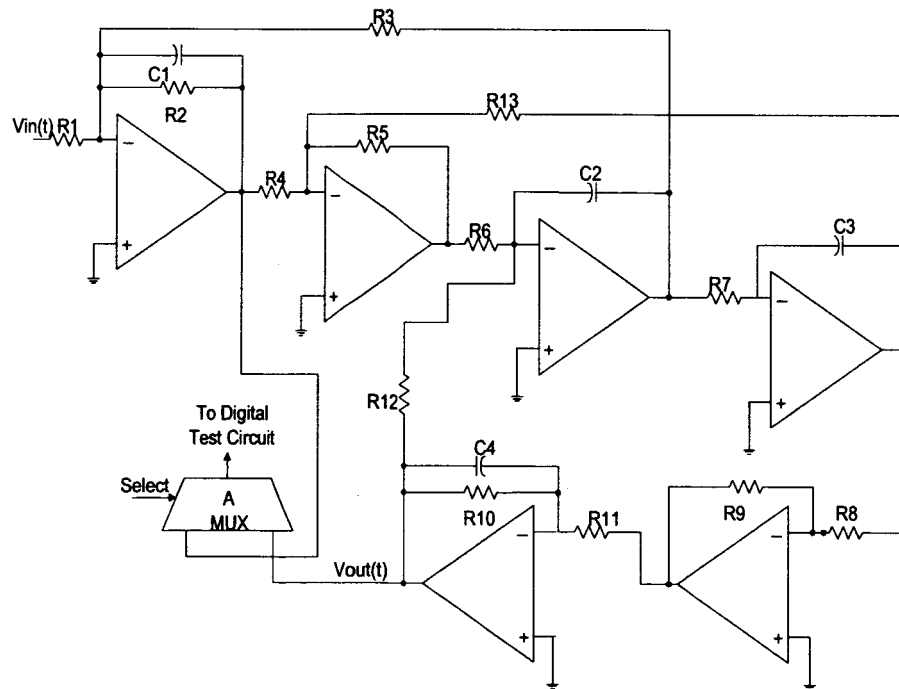


Figure 15 ITC'97 Leap-Frog Filter

response of this filter at outputs $V_{out1}(t)$ and $V_{out2}(t)$ is,

$$\begin{aligned} V_{out1}(t) &= V_{DD}K_1e^{-\alpha t} \left[\cos\left[\sqrt{\beta-\alpha^2}t\right] - \frac{\alpha}{\sqrt{\beta-\alpha^2}}\sin\left[\sqrt{\beta-\alpha^2}t\right] \right] u(t), \quad \beta > \alpha^2 \\ V_{out2}(t) &= \frac{V_{DD}K_1K_2}{\beta} \left\{ 1 - e^{-\alpha t} \left[\cos\left[\sqrt{\beta-\alpha^2}t\right] + \frac{\alpha}{\sqrt{\beta-\alpha^2}}\sin\left[\sqrt{\beta-\alpha^2}t\right] \right] \right\} u(t), \quad \beta > \alpha^2. \end{aligned} \quad (8)$$

We considered one case here i.e. $\beta > \alpha^2$ and are not expressing the variables in eq. (8) in terms of the circuit element values for brevity. These two output signals can be used to realized a component function similar to eq.

approach that is based upon the step response of the analog CUT. Although, this technique posses many of the characteristics of fault based BIST techniques such as using non-conventional stimuli and CUT output measurements it is also like functional BIST techniques

Table 2: Proposed BIST Approach Convergence Behavior for Benchmark Circuits

Circuit	Soft Fault	No. Parameters	No. Iteration	Error
Continuous-time State-variable filter [7]	-6 σ	4	25	0.017
	+6 σ	4	25	0.28
Leap-frog filter [7]	-6 σ	9	19	10 ⁻⁷
	+6 σ	9	25	0.1659
Elliptical filter [1]	-6 σ	14	25	0.001
	+6 σ	14	25	0.21

(5) that is a function of the following four parameters α , β , K_1 and K_2 . These parameters are required to find the transfer function of the above filter. The Jacobin matrix, i.e. a matrix similar to eq. (6), required to find these parameters using the Newton method can be realized with this component function and eight crossover points. These crossover points correspond to the points in time when the outputs of the CUT equal to four reference voltages that are set in the digital test circuit. The nominal parameter values are used for the initial values of the Newton algorithm. The Newton algorithm converged for the two soft fault cases sited in [7], i.e. nominal plus 6 σ case and nominal minus 6 σ case. Similar results were found for the Leap-frog filter shown in Fig. 5 and the Elliptical filter shown in Fig. 6. The number of unknown parameters associated with each of these filters and the iteration count required to reduce the Newton loop error function to 10⁻⁶ or reach the loop limit, i.e. 25, is shown in Table 2.

in the sense that it can be used to detect both hard and soft faults. The CUT excitation circuit can be realized with digital techniques because of the above property and the time domain based realization of the proposed BIST technique. The test measurements are acquired with a digital circuit, and processed with a finite-state machine to construction and solve the matrix $\mathbf{J}(\mathbf{x})$ to implement the Newton-Raphson equations. The proposed technique is effective under process drift because of these models. The technique is also insensitive to the initial state of the CUT and the switching voltage of the circuit driven by the CUT. The number of reference voltages required to implement this approach must equals the number of circuit unknowns. These references do not need to be known or precise. The CUT needs to be reconfigurable or needs to contain multiple outputs. The output of each configuration or output for the multiple output case must overlap to construct the component functions.

4. Conclusion

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